WHAT IS CLAIMED IS:

1. A method for forming a multi-level interconnection structure in a semiconductor device, said method comprising the steps of:

forming first level interconnections overlying a substrate;

consecutively forming first and second dielectric films on said first level interconnections;

consecutively forming first through third mask films on said second dielectric film, said first through third hard mask films being insulating films and having different etching rates in an etching condition;

selectively etching said second and third hard mask films to form a through-hole pattern on said second and third hard mask films;

selectively etching said third hard mask film to form a trench pattern on said third hard mask film, said trench pattern partially overlapping said through-hole pattern;

selectively etching said first hard mask film by using said second hard mask film as an etching mask to form said through-hole pattern on said first hard mask film;

selectively etching said second dielectric film by using said first hard mask film as an etching mask to form first through-holes in said second dielectric film based on said through-hole pattern;

selectively etching said first and second hard mask films and a top portion of said first dielectric film by using said third hard

mask film as an etching mask to form trenches in said first and second hard mask films and said top portion of said second dielectric film based on said trench pattern; and

selectively etching said first dielectric film to form therein second through-holes communicated with respective said first through-holes for exposing part of said first level interconnections through said first and second through-holes.

2. The method as defined in claim 1, wherein said second dielectric film has a three-layer structure including a first low-permittivity layer, an etch stop layer and a second low-permittivity layer consecutively formed on said first dielectric film.

3. The method as defined in claim 2, wherein said trenches have a bottom surface implemented by a top surface of said etch stop layer.

4. The method as defined in claim 1, wherein said second dielectric film has a two-layer structure including an etch stop layer and a low-permittivity layer overlying said etch stop layer.

5. The method as defined in claim 4, wherein said trenches have a bottom surface implemented by a top surface of said etch stop layer.

6. The method as defined in claim 1, wherein said first hard mask film is made of a material same as a material of said first dielectric film.

7. The method as defined in claim 1, further comprising the step of forming a first anti-reflection film on top of said third hard mask film.

8. The method as defined in claim 7, further comprising, between said selectively etching step of said second and third hard mask films and said selectively etching step of said third hard mask film, the steps of removing said first anti-reflection film and forming a second anti-reflection film on said third hard mask film,.

9. The method as defined in claim 1, wherein said first dielectric film is an anti-diffusion film for suppressing diffusion of said first level interconnections.

10. The method as defined in claim 1, wherein said first level interconnections, said first hard mask film, said second hard mask film and said third hard mask film are made of Cu, SiC, SiO_2 and SiN, respectively.

11. A semiconductor device comprising a substrate, first level interconnections overlying said substrate, first and second dielectric

films consecutively formed on said first level interconnections, third through fifth dielectric films having different compositions from one another, said third through fifth dielectric films and at least a top portion of said second dielectric films defining interconnection trenches therein, said first through fifth dielectric films having through-holes penetrating therethrough, second level interconnections formed in said interconnection trenches, and via holes for filling said through-holes to connect said first level interconnections to said second level interconnections.

12. The semiconductor device as defined in claim 11, wherein said first dielectric film is an anti-diffusion film for suppressing diffusion of said first level interconnections.

13. The semiconductor device as defined in claim 11, wherein said first level interconnections, said third dielectric film, said fourth dielectric film and said fifth dielectric film are made of Cu, SiC, SiO_2 and SiN, respectively.